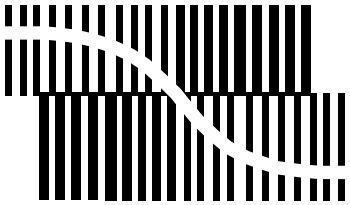
DATA SHEET



UDA1334ATS
Low power audio DAC with PLL

Product specification
Supersedes data of 2000 Feb 09

2000 Jul 31

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1 FEATURES

1.1 General

- 2.4 to 3.6 V power supply voltage
- On-board PLL to generate the internal system clock:
  - Operates as an asynchronous DAC, regenerating the internal clock from the WS signal (called audio mode)
  - Generates audio related system clock (output) based on 32, 48 or 96 kHz sampling frequency (called video mode).
- Integrated digital filter plus DAC
- Supports sample frequencies from 16 to 100 kHz in asynchronous DAC mode
- No analog post filtering required for DAC
- Easy application
- SSOP16 package.

1.2 Multiple format data interface

- I^2S-bus and LSB-justified format compatible
- $1f_s$ input data rate.

1.3 DAC digital features

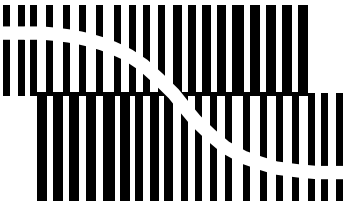
- Digital de-emphasis for 44.1 kHz sampling frequency
- Mute function.

1.4 Advanced audio configuration

- High linearity, wide dynamic range and low distortion.

1.5 PLL system clock generation

- Integrated low jitter PLL for use in applications in which there is digital audio data present but the system cannot provide an audio related system clock. This mode is called audio mode.
- The PLL can generate 256 × 48 kHz and 384 × 48 kHz from a 27 MHz input clock. This mode is called video mode.



2 APPLICATIONS

This audio DAC is excellently suitable for digital audio portable application, specially in applications in which an audio related system clock is not present.

3 GENERAL DESCRIPTION

The UDA1334ATS is a single chip 2 channel digital-to-analog converter employing bitstream conversion techniques, including an on-board PLL. The extremely low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates a playback function.

The UDA1334ATS supports the I^2S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334ATS has basic features such as de-emphasis (44.1 kHz sampling frequency, only supported in audio mode) and mute.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1334ATS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	DAC analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
I_{DDA}	DAC analog supply current	audio mode	–	3.5	–	mA
		video mode	–	3.5	–	mA
I_{DDD}	digital supply current	audio mode	–	2.5	–	mA
		video mode	–	4.5	–	mA
T_{amb}	ambient temperature		−40	–	+85	°C
Digital-to-analog converter (V_{DDA} = V_{DDD} = 3.0 V)						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	–	900	–	mV
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	–	−90	–	dB
		f_s = 44.1 kHz; at −60 dB; A-weighted	–	−40	–	dB
		f_s = 96 kHz; at 0 dB	–	−85	–	dB
		f_s = 96 kHz; at −60 dB; A-weighted	–	−38	–	dB
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	–	100	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	98	–	dB
α_{CS}	channel separation		–	100	–	dB
Power dissipation (at f_s = 44.1 kHz)						
P	power dissipation	audio mode	–	18	–	mW
		video mode	–	24	–	mW

Note

1. The output voltage of the DAC scales proportionally to the power supply voltage.

6 BLOCK DIAGRAM

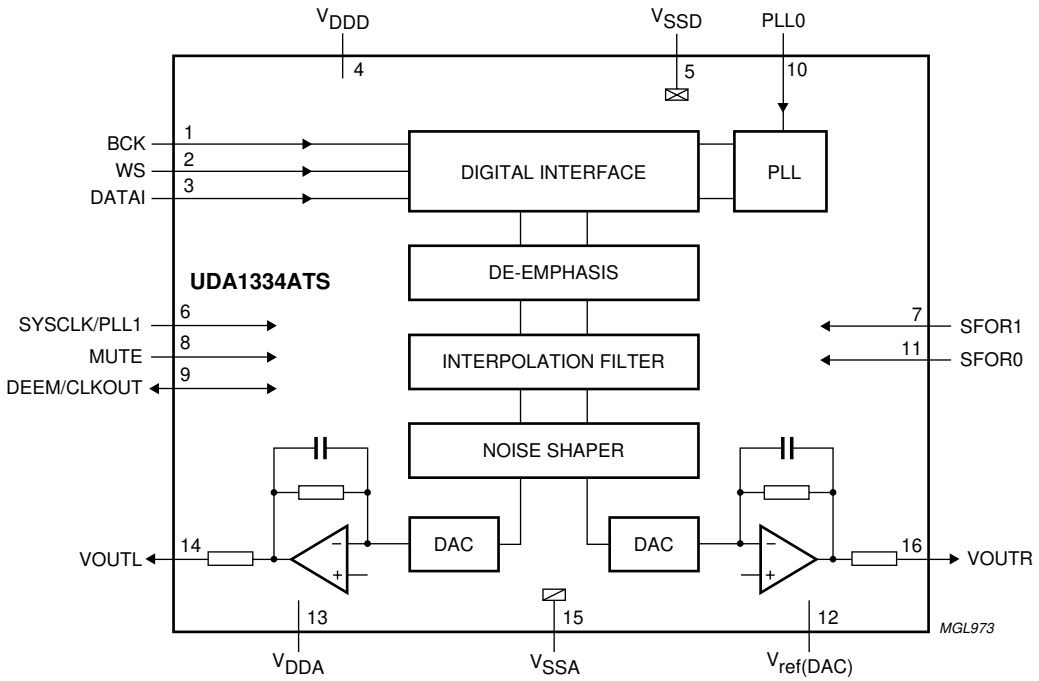


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	PAD TYPE	DESCRIPTION
BCK	1	5 V tolerant digital input pad	bit clock input
WS	2	5 V tolerant digital input pad	word select input
DATAI	3	5 V tolerant digital input pad	serial data input
V_{DDD}	4	digital supply pad	digital supply voltage
V_{SSD}	5	digital ground pad	digital ground
SYSCLK/PLL1	6	5 V tolerant digital input pad	system clock input in video mode/PLL mode control 1 input in audio mode
SFOR1	7	5 V tolerant digital input pad	serial format select 1 input
MUTE	8	5 V tolerant digital input pad	mute control input
DEEM/CLKOUT	9	5 V tolerant digital input/output pad	de-emphasis control input in audio mode/clock output in video mode
PLL0	10	3-level input pad; note 1	PLL mode control 0 input
SFOR0	11	digital input pad; note 1	serial format select 0 input
$V_{ref(DAC)}$	12	analog pad	DAC reference voltage
V_{DDA}	13	analog supply pad	DAC analog supply voltage
VOUTL	14	analog output pad	DAC output left
V_{SSA}	15	analog ground pad	DAC analog ground
VOUTR	16	analog output pad	DAC output right

Note

1. Because of test issues these pads are not 5 V tolerant and both pads should be at power supply voltage level or at a maximum of 0.5 V above that level.

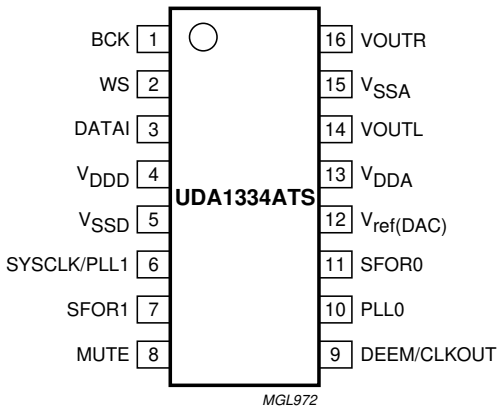


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1334ATS incorporates a PLL capable of generating the system clock. The UDA1334ATS can operate in 2 modes:

- It operates as an asynchronous DAC, which means the device regenerates the internal clocks using a PLL from the incoming WS signal. This mode is called audio mode.
- It generates the internal clocks from a 27 MHz clock input, based on 32, 48 and 96 kHz sampling frequencies. This mode is called video mode.

In video mode, the digital audio input is slave, which means that the system must generate the BCK and WS signals from the output clock available at pin CLKOUT of the UDA1334ATS. The digital audio signals should be frequency locked to the CLKOUT signal.

Remarks:

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface
2. For LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

8.1.1 AUDIO MODE

Audio mode is enabled by setting pin PLL0 to LOW. De-emphasis can be activated via pin DEEM/CLKOUT according to Table 5.

In audio mode, pin SYSCLK/PLL1 is used to set the sampling frequency range as given in Table 1.

Table 1 Sampling frequency range in audio mode

SYSCLK/PLL1	SELECTION
LOW	f_s = 16 to 50 kHz
HIGH	f_s = 50 to 100 kHz

8.1.2 VIDEO MODE

In video mode, the master clock is a 27 MHz external clock (as is available in video environment). A clock-out signal is generated at pin DEEM/CLKOUT. The output frequency can be selected using pin PLL0. The output frequency is either 12.228 MHz (256 × 48 kHz) with pin PLL0 being at MID level or 18.432 MHz (384 × 48 kHz) with pin PLL0 being HIGH, as given in Table 2.

Table 2 Clock output selection in video mode

PLL0	SELECTION
MID	12.228 MHz clock; note 1
HIGH	18.432 MHz clock; note 2
LOW	audio mode

Notes

1. The supported sampling frequencies are: 96, 48 and 24 kHz or 64, 32 and 16 kHz.
2. The supported sampling frequencies are: 96, 48 and 24 kHz; 72 and 36 kHz or 32 kHz.

8.2 Interpolation filter

The interpolation digital filter interpolates from $1f_s$ to $64f_s$ by cascading FIR filters (see Table 3).

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	$0f_s$ to $0.45f_s$	±0.02
Stop band	$>0.55f_s$	−50
Dynamic range	$0f_s$ to $0.45f_s$	>114

8.3 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

8.4 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally to the power supply voltage.

8.5 Power-on reset

The UDA1334ATS has an internal Power-on reset circuit (see Fig.3) which resets the test control block.

The reset time (see Fig.4) is determined by an external capacitor which is connected between pin $V_{ref(DAC)}$ and ground. The reset time should be at least 1 μs for $V_{ref(DAC)} < 1.25$ V. When V_{DDA} is switched off, the device will be reset again for $V_{ref(DAC)} < 0.75$ V.

During the reset time the system clock should be running.

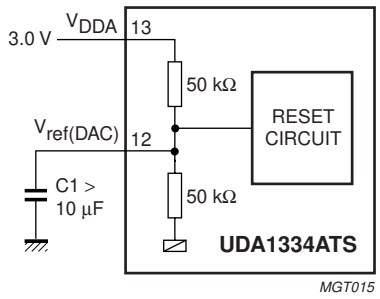


Fig.3 Power-on reset circuit.

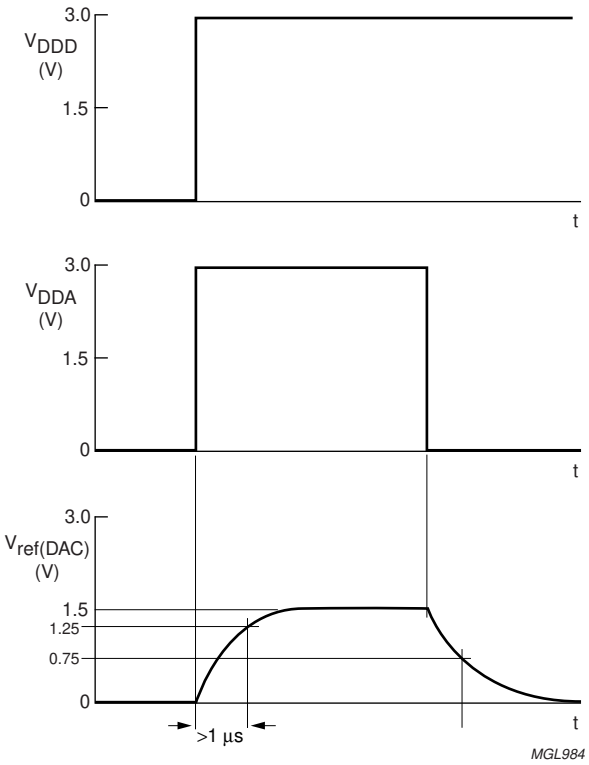


Fig.4 Power-on reset timing.

8.6 Feature settings

8.6.1 DIGITAL INTERFACE FORMAT SELECT

The digital audio interface formats (see Fig.5) can be selected via pins SFOR1 and SFOR0 as shown in Table 4.

For the digital audio interface holds that the BCK frequency can be maximum 64 times WS frequency.

The WS signal must change at the negative edge of the BCK signal for all digital audio formats.

Table 4 Data format selection

SFOR1	SFOR0	INPUT FORMAT
LOW	LOW	I^2S-bus input
LOW	HIGH	LSB-justified 16 bits input
HIGH	LOW	LSB-justified 20 bits input
HIGH	HIGH	LSB-justified 24 bits input

8.6.2 DE-EMPHASIS CONTROL

This function is only available in audio mode. In that case, pin DEEM/CLKOUT can be used to activate the digital de-emphasis for 44.1 kHz as given in Table 5.

Table 5 De-emphasis control (audio mode)

DEEM/CLKOUT	FUNCTION
LOW	de-emphasis off
HIGH	de-emphasis on

8.6.3 MUTE CONTROL

The output signal can be soft muted by setting pin MUTE to HIGH as given in Table 6.

Table 6 Mute control

MUTE	FUNCTION
LOW	mute off
HIGH	mute on

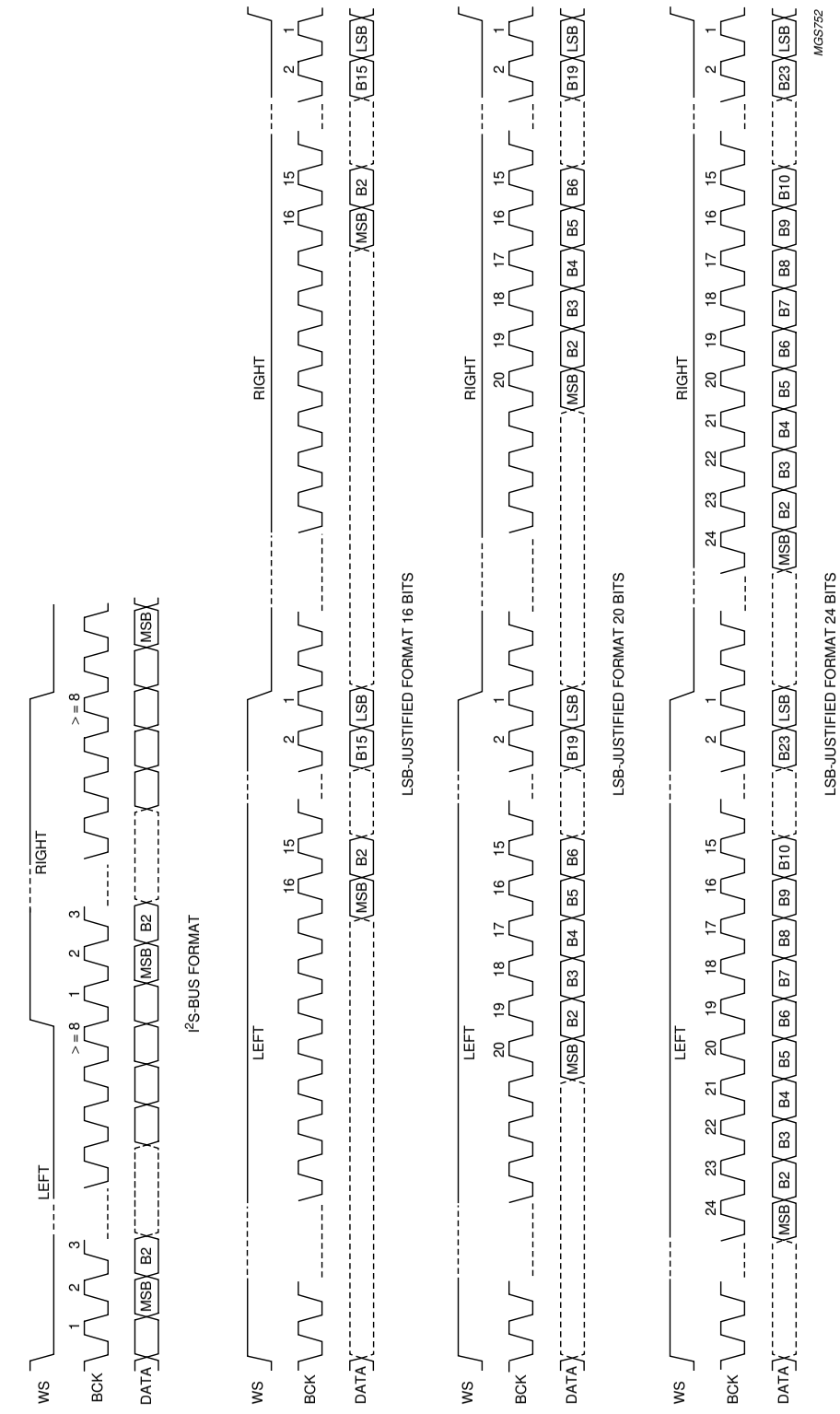


Fig.5 Digital audio formats.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	4.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		−65	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{es}	electrostatic handling voltage	human body model; note 2	−2000	+2000	V
		machine model; note 2	−250	+250	V
$I_{sc(DAC)}$	short-circuit current of DAC	note 3			
		output short-circuited to V_{SSA}	–	450	mA
		output short-circuited to V_{DDA}	–	300	mA

Notes

1. All supply connections must be made to the same power supply.
2. ESD behaviour is tested according to JEDEC II standard.
3. Short-circuit test at T_{amb} = 0 °C and V_{DDA} = 3 V. DAC operation after short-circuiting cannot be warranted.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	145	K/W

12 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*.

13 DC CHARACTERISTICS

V_{DDD} = V_{DDA} = 3.0 V; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	DAC analog supply voltage	note 1	2.4	3.0	3.6	V
V_{DDD}	digital supply voltage	note 1	2.4	3.0	3.6	V
I_{DDA}	DAC analog supply current	audio mode	–	3.5	–	mA
		video mode	–	3.5	–	mA
I_{DDD}	digital supply current	audio mode	–	2.5	–	mA
		video mode	–	4.5	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pins: TTL compatible						
V_{IH}	HIGH-level input voltage		2.0	–	5.0	V
V_{IL}	LOW-level input voltage		−0.5	–	+0.8	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
3-level input: pin PLL0						
V_{IH}	HIGH-level input voltage		$0.9V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IM}	MID-level input voltage		$0.4V_{DDD}$	–	$0.6V_{DDD}$	V
V_{IL}	LOW-level input voltage		−0.5	–	+0.5	V
Digital output pins						
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
DAC						
$V_{ref(DAC)}$	reference voltage	with respect to V_{SSA}	$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V
$R_{o(ref)}$	output resistance on pin $V_{ref(DAC)}$		–	25	–	kΩ
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%; R_L = 5 kΩ	–	1.6	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	50	pF

Notes

1. All supply connections must be made to the same external power supply unit.
2. When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

14 AC CHARACTERISTICS

14.1 Analog

V_{DDD} = V_{DDA} = 3.0 V; f_i = 1 kHz; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
DAC				
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	900	mV
ΔV_o	unbalance between channels		0.1	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	−90	dB
		f_s = 44.1 kHz; at −60 dB; A-weighted	−40	dB
		f_s = 96 kHz; at 0 dB	−85	dB
		f_s = 96 kHz; at −60 dB; A-weighted	−38	dB

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	100	dB
		f_s = 96 kHz; code = 0; A-weighted	98	dB
α_{CS}	channel separation		100	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 30 mV (p-p)	60	dB

Note

1. The output voltage of the DAC scales proportionally to the analog power supply voltage.

14.2 Timing

$V_{DDD} = V_{DDA}$ = 2.4 to 3.6 V; T_{amb} = −20 to +85 °C; R_L = 5 kΩ; all voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output clock timing in video mode (see Fig.6)						
T_{sys}	output clock cycle	f_o = 12.228 MHz	–	81.38	–	ns
		f_o = 18.432 MHz	–	54.25	–	ns
t_{CWL}	output clock LOW time	f_o = 12.228 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		f_o = 18.432 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
t_{CWH}	output clock HIGH time	f_o = 12.228 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		f_o = 18.432 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
Serial input data timing (see Fig.7)						
f_{BCK}	bit clock frequency		–	–	$64f_s$	Hz
t_{BCKH}	bit clock HIGH time		50	–	–	ns
t_{BCKL}	bit clock LOW time		50	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(DATAI)}$	set-up time data input		20	–	–	ns
$t_{h(DATAI)}$	hold time data input		0	–	–	ns
$t_{su(WS)}$	set-up time word select		20	–	–	ns
$t_{h(WS)}$	hold time word select		10	–	–	ns

Note

1. The typical value of the timing is specified for a sampling frequency of 44.1 kHz.

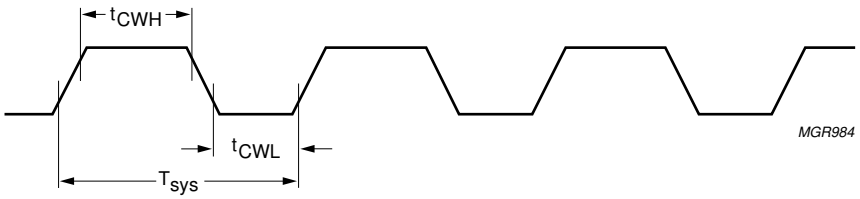


Fig.6 Output clock timing.

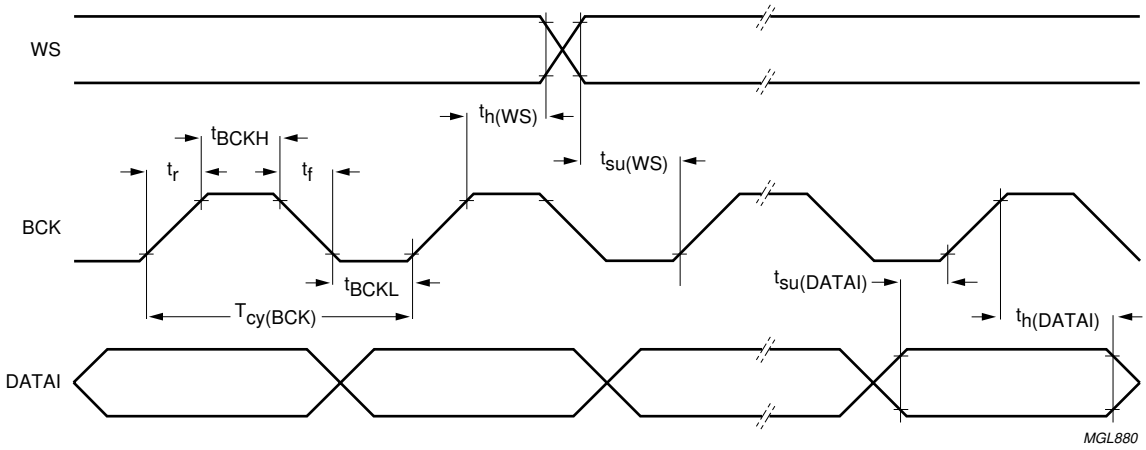
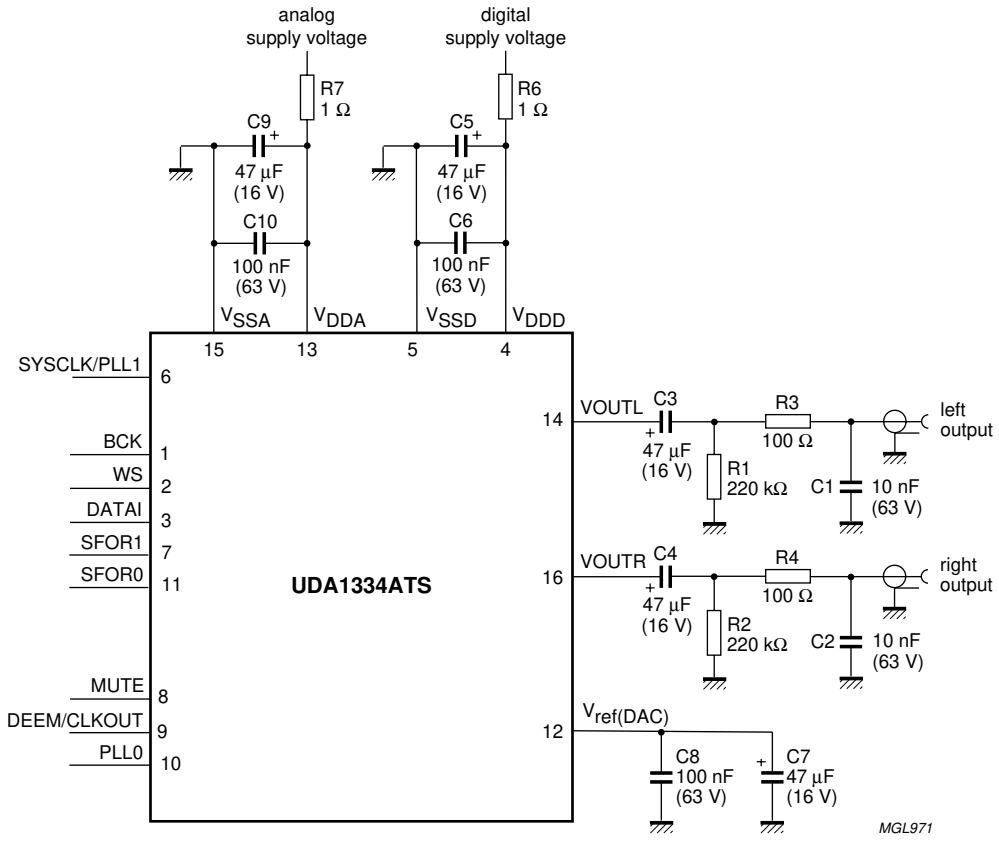


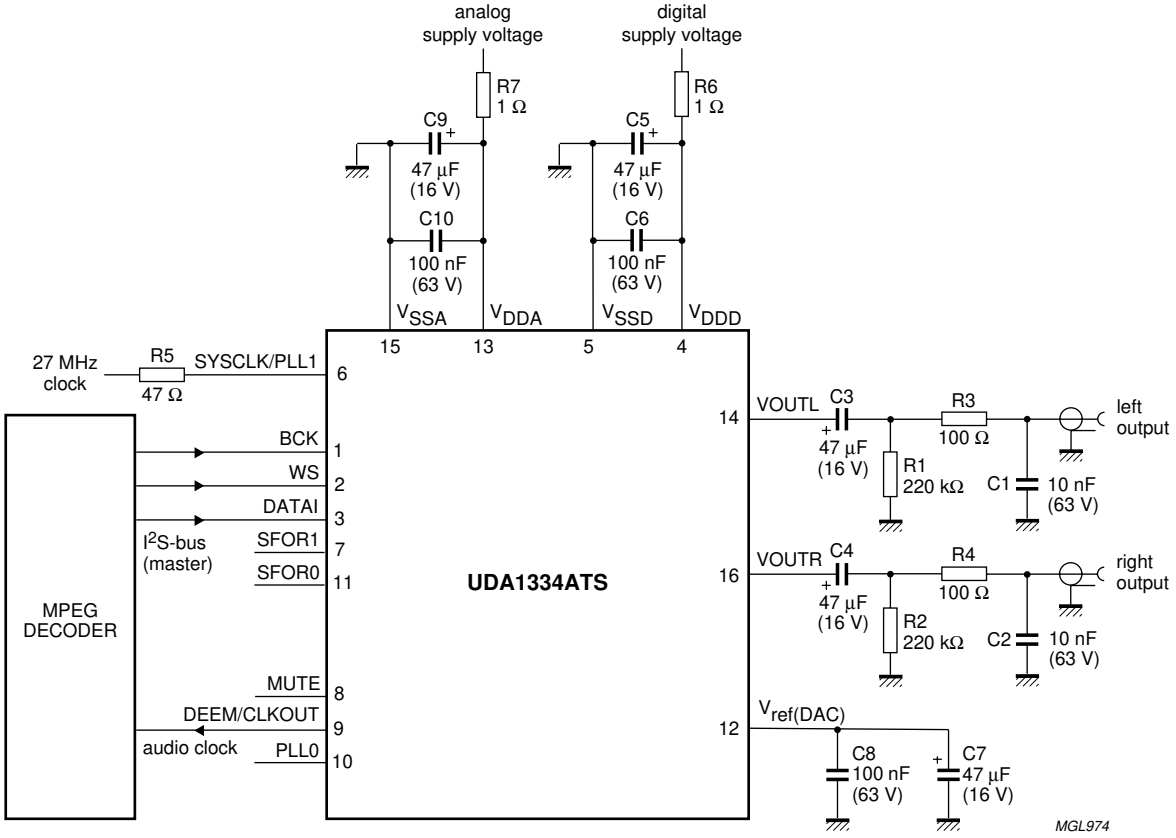
Fig.7 Serial interface timing.

15 APPLICATION INFORMATION



In audio mode, the system does not need to supply a system clock.

Fig.8 Audio mode application diagram.

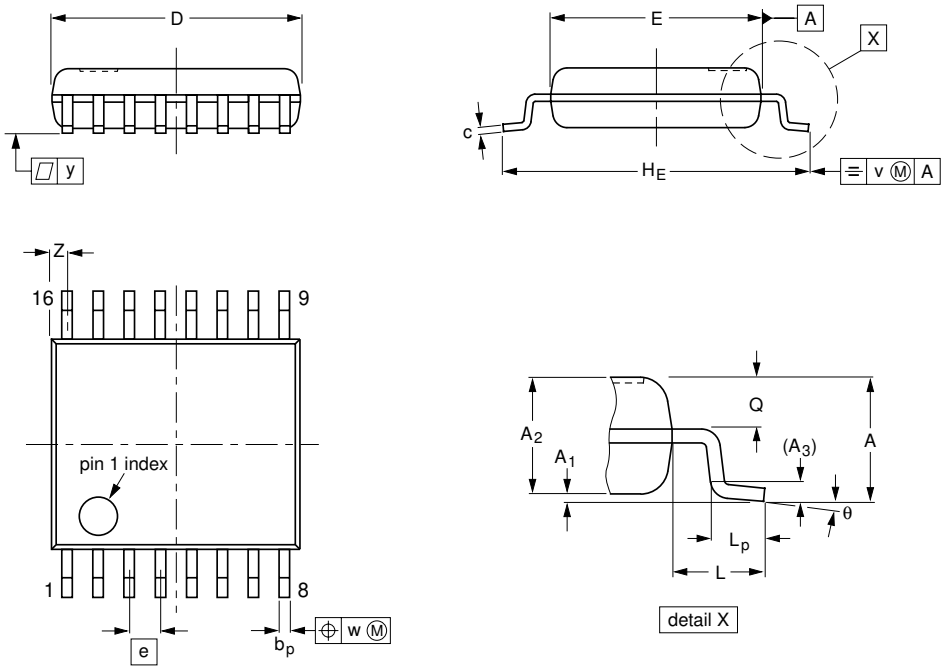


In video mode, a clock output signal is generated by the UDA1334ATS which is master for the audio signals in the system; the digital audio interface is slave, which means the system must generate the BCK and WS signal from the UDA1334ATS output clock.

Fig.9 Video mode application diagram.

16 PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.3 5.1	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT369-1		MO-152				~~99-12-27~~ 03-02-19

17 SOLDERING

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

18 DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

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